

TIME-VARIANT CIC-FILTERS FOR SAMPLE RATE CONVERSION WITH ARBITRARY RATIONAL FACTORS

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ABSTRACT

Sample rate conversion (SRC) with rational factors can be realized by interpolation followed by decimation, where CIC-Filters [1] can be chosen for either. However, the necessary increase of the sample rate that goes with the interpolation is not feasible in most RF-applications. Therefore a time-variant implementation of CIC-filters is presented which circumvents the high intermediate sample rate. This time-variant implementation results in a linear periodically time-variant system (LPTV) which is completely equivalent to its original linear time-invariant system (LTI) consisting of the interpolator and the decimator. Thus well-known methods of system analysis can be used by analysing the LTI system, while implementing the system as an LPTV system, avoiding the high intermediate sample rates of the LTI system. The advantage of CIC-filters not having stored the coefficients of the impulse response but rather the description of the impulse response, enabling an implementation which is independent of the interpolation- as well as the decimation-factor, is preserved with the LPTV system. In contrast to Lagrange interpolators cancelling only the image components of the interpolated signal, time-variant CIC-filters also cancel the aliasing components, which is important in applications, where anti-aliasing is more important than anti-imaging.

1. INTRODUCTION

In many applications sample-rate conversion has to be performed in an adaptable manner, i.e. the rate change factor has to be adapted to the current application of the device. An example is the sample-rate adaptation in multi-mode mobile communications receivers, where depending on the current standard of operation different symbol rates are required while the analog-to-digital converter (ADC) samples the input signal at a fixed rate. In such receivers the application of Sigma-Delta modulators ($\Sigma\Delta$ -M) as ADC has advantages compared to classical memoryless ADCs [2]. Therefore Sigma-Delta modulated signals will serve as input signals to the investigated sample rate converters.

To get a software adaptable sample rate converter based on a fixed hardware conventional polyphase structures with the number of branches depending on the

rate change factor cannot be used. Hence a one-branch-structure has to be used, which is given in fig. 1.

Especially in RF-applications, where the signals are sampled at very high rates, increasing the input sample rate due to interpolation (see fig. 1) is not feasible. In the following we show that in connection with CIC-filters this can be avoided.

2. CIC-FILTERS FOR INTERPOLATION AND DECIMATION

CIC-filters are linear phase FIR-filters which have been thoroughly discussed in [1]. For completeness their structure is given in fig. 2. The CIC-filter realizes a moving average calculation of the order N . The frequency response of the filter is

$$H(F) = \left(\frac{\sin(\pi RF)}{\sin(\pi F)} \right)^N e^{-j(R-1)NF} \quad (1)$$

with $0 \leq F = fT < 1$ and $R = KL$ or KM , $K \in \{1, 2\}$

Hence it suppresses aliasing or imaging errors, respectively. Because of its simplicity it is often used for over-sampled narrowband signals.

3. MODIFIED CIC-FILTERS

A cascade of interpolator and decimator requires an intermediate clock rate which is higher than input sample rate. Since only the integrator section is operating at this high intermediate sampling rate it should be merged with the up- and down-sampler to a time-variant unit which is clocked only at input sampling rate f_{in} . Two facts are used: on the one hand up-sampling means just filling in $L - 1$ zero pads between each pair of input samples and on the other hand down-sampling means picking up every M th value of the signal at the output of the filter. While calculating only the necessary intermediate steps, up-sampling can be done virtually.

With up-sampling $L \uparrow$ we will get $x^{**}(kL + \varrho)$ as input signal to the integrator section.

$$x^{**}(kL + \varrho) = \begin{cases} x^*(k) & \text{for } \varrho = 0 \\ 0 & \text{for } \varrho = 1, 2, \dots, L - 1 \end{cases} \quad (2)$$

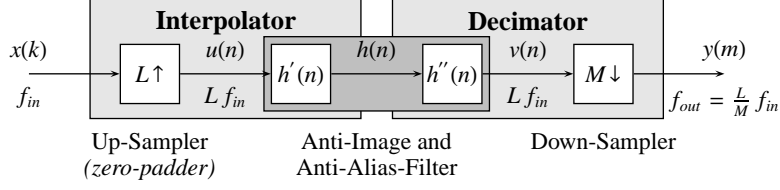


Fig. 1: Direct digital approach for a sample rate converter with arbitrary rational factors as a cascade of interpolator and decimator

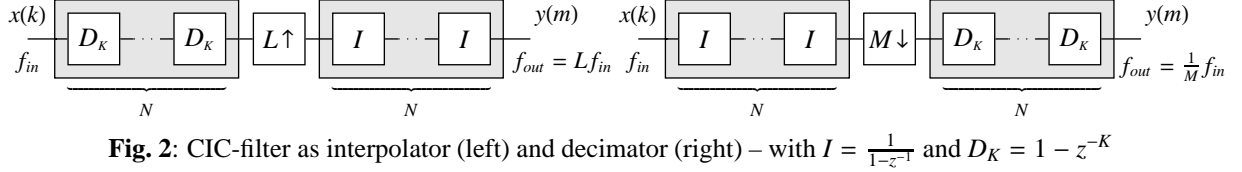


Fig. 2: CIC-filter as interpolator (left) and decimator (right) – with $I = \frac{1}{1-z^{-1}}$ and $D_K = 1 - z^{-K}$

Calculating the state-space form we get the state equation (clock rate Lf_{in} and $0 \leq \varrho \leq L - 1$) as

$$\begin{pmatrix} z_1(kL + 1 + \varrho) \\ z_2(kL + 1 + \varrho) \\ \vdots \\ z_N(kL + 1 + \varrho) \end{pmatrix} = \begin{pmatrix} 1 & 0 & \cdots & 0 \\ 1 & 1 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 1 & 1 & \cdots & 1 \end{pmatrix}^{\varrho+1} \begin{pmatrix} z_1(kL) \\ z_2(kL) \\ \vdots \\ z_N(kL) \end{pmatrix} + \begin{pmatrix} 1 & 0 & \cdots & 0 \\ 1 & 1 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 1 & 1 & \cdots & 1 \end{pmatrix}^{\varrho} \begin{pmatrix} 1 \\ 1 \\ \vdots \\ 1 \end{pmatrix} (x^{**}(kL)) \quad (3)$$

and the output map as

$$y^{**}(kL + \varrho) = y^*\left(k + \frac{\varrho}{L}\right) = z_N(kL + 1 + \varrho) \quad (4)$$

Since we are merely interested in the output samples $y(m) = y(k + \frac{\varrho}{L})$ eq. (3,4) can be transferred to clock rate f_{in} , and get thus a much simpler form

$$\begin{pmatrix} z_1(k+1) \\ z_2(k+1) \\ \vdots \\ z_N(k+1) \end{pmatrix} = \begin{pmatrix} L_{1,1} & L_{1,2} & \cdots & L_{1,N} \\ L_{2,1} & L_{2,2} & \cdots & L_{2,N} \\ \vdots & \vdots & \ddots & \vdots \\ L_{N,1} & L_{N,2} & \cdots & L_{N,N} \end{pmatrix} \begin{pmatrix} z_1(k) + x^*(k) \\ z_2(k) \\ \vdots \\ z_N(k) \end{pmatrix} \quad (5)$$

$$y^*(m) = y^*\left(k + \frac{\varrho(m)}{L}\right) \quad (6)$$

$$= \begin{pmatrix} \varrho_{N-1}(m) & \varrho_{N-2}(m) & \cdots & 1 \end{pmatrix} \begin{pmatrix} z_1(k) + x^*(k) \\ z_2(k) \\ \vdots \\ z_{N-1}(k) \\ z_N(k) \end{pmatrix}$$

with

$$L_{i,j} = \begin{cases} \frac{(N-j)! (L-1+i-j)!}{(N-i)! (i-j)! (L-1)!} \in \mathbb{N} & \text{for } i > j \\ 1 & \text{for } i = j \\ 0 & \text{for } i < j \end{cases} \quad (7)$$

$$\varrho_i(m) = \prod_{h=1}^i \varrho(m) + h \quad (8)$$

The coefficients $L_{i,j}$ have to be calculated only once just before setting up the sample rate converter. Meanwhile the coefficients $\varrho_i(m)$ are time-varying and have to be calculated for every output sample $y(m)$ at run-time. So for simplifying $\varrho_i(m)$ the eq. (5-8) are already including a similarity transformation. Eq. (5,6) suggest a structure for the SRC which can be seen in fig. 3.

While interpreting the state-space equations we realize that the first stage of the modified integrator section is a simple integrator which is clocked at the same rate as the interpolator comb section. That means for $N_I \geq 1$ we can cancel the first integrator stage together with the last comb stage of the interpolator and therefore decrease the number of operations. While choosing $N_I = 1$ and using a 1-bit $\Sigma\Delta$ -M as ADC we preserve the advantage of a 1-bit input signal and can replace the multipliers $L_{i,1}$ by simple switchable registers.

It must be stressed that a CIC filter is not completely equivalent to a moving average FIR filter because having a feedback structure the integrator stages have poles in $z = 1$ ($\Omega = 0$) which are compensated by zeros of the same order of the comb stages. This results a possibly unlimited increasing of the accumulated values and therefore in register overflow but is of no consequence if the following two conditions are met. 1) The filter has to be implemented with two's complement arithmetic or an other "wrap around logic", and 2) the range of number systems is greater or equal the expected maximum magnitude at the output $y(m)$ of the filter [1]. All registers have to be implemented with the same word length w_{out} while rounding and truncation in the lower significant bits is still possible. The necessary word length can be calculated to

$$w_{out} \geq \left[(N_I - 1) \text{ld}(L) + N_D \text{ld}(KM) + \text{ld}((N_D + N_I - 1)!) \right] + w_{in} \quad (9)$$

The only remaining problem is how to evaluate the correct clock for generating a new output sample $y(m)$ and the correct value of $\varrho(m)$. For controlling of both prob-

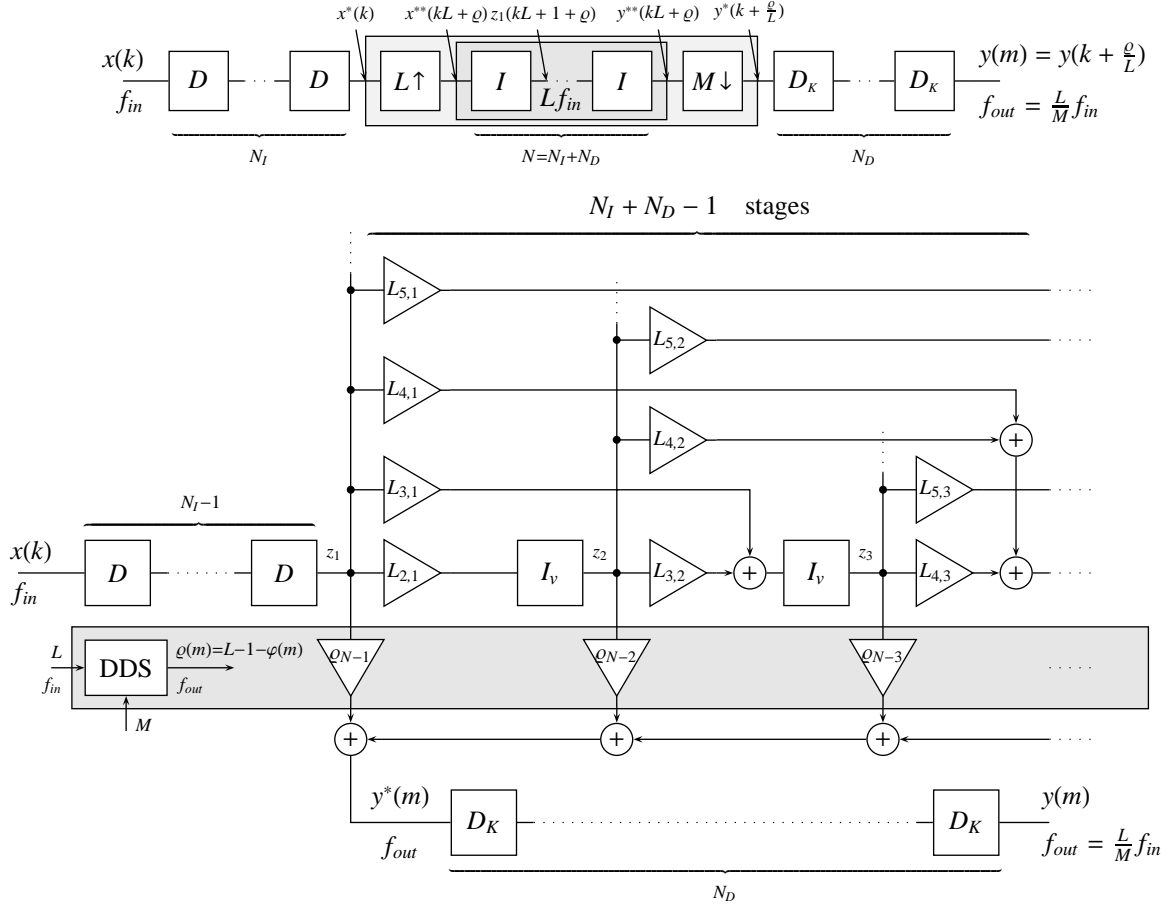


Fig. 3: Time-variant CIC-filters (bottom) for sample rate conversion with arbitrary rational factors (with $I = \frac{1}{1-z^{-1}}$, $I_v = Iz^{-1}$, $D = 1 - z^{-1}$) and equivalent cascade (top)

lems we can take a simple variable accumulator which is overflowing at M and headed with L ($L < M$) at the clock rate f_{in} as DDS. An overflow indicates that a new output sample has to be generated and the remainder $\varphi(m)$ in accumulator gives the needed $\varrho(m) = L - 1 - \varphi(m)$. Obviously, the accumulator generates a jittered clock with a mean frequency $f_{out} = \frac{L}{M}f_{in}$ and causes the calculation of output samples. This jitter can be eliminated by means of buffering the output samples in a register.

The DDS output signal $\varphi(m)$ which are the remainders after overflow will also be used for generating the coefficients $\varrho_i(m)$ and a resulting structure can be seen in fig. 4.

4. MULTIPLIER-FREE STRUCTURES

For input signals comprising only the values $\{-1,0,1\}$ the multipliers can be replaced by switchable registers. The output signal of a 1-bit Sigma-Delta modulator is such an input signal. Hence under certain circumstances the sampling rate converter with modified CIC filters can be simplified to a multiplier free structure. This is possible when choosing $N_I = N_D = 1$ (first order rejection of aliasing and imaging errors). The resulting SRC is given in fig. 5.

For the register growth we get

$$\begin{aligned} wl_{in} &= 2 \quad (1 \text{ bit SDM} + \text{sign}) - \text{ternary code} \\ wl_{out} &= \lceil \text{ld}(KM) \rceil + 1 \end{aligned} \quad (10)$$

5. RESULTS

Simulation results with an $\Sigma\Delta$ -M as input signal source are shown in fig. 6. It can clearly be seen that the $\Sigma\Delta$ -M noise shaping curve is not destroyed by the sample rate conversion process, in accordance to [3], where ordinary CIC-decimators are used for decimation of $\Sigma\Delta$ modulated signals. Independently from the choice of L and M it is possible to put zeros of the order N_I or N_D at the center of the imaging or potential aliasing bands, respectively. Hence no signal distortion will occur for $\Omega = 0$ and only a slowly increasing aliasing distortion for $\Omega > 0$ will happen. But on the other hand the quantization noise will always hide this aliasing distortion under the condition of a particular order N_D which is greater or equal the order of the $\Sigma\Delta$ -M [3]. That also means that the use of a $\Sigma\Delta$ -M with an order greater than N_D is without any advantages because the level of aliasing distortion will be greater than the power of the quantization noise of the $\Sigma\Delta$ -M.

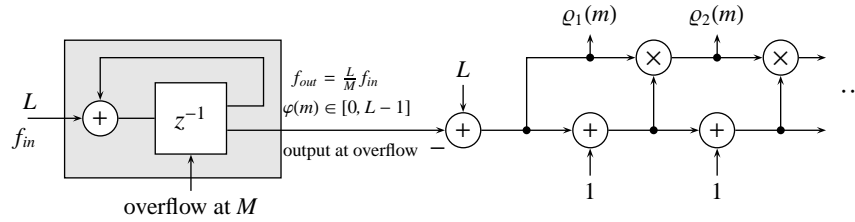


Fig. 4: Control unit for modified CIC filters

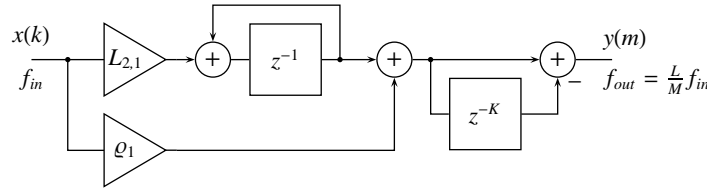
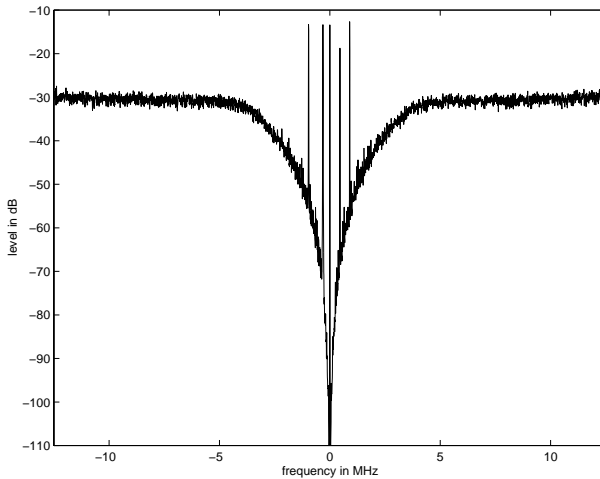
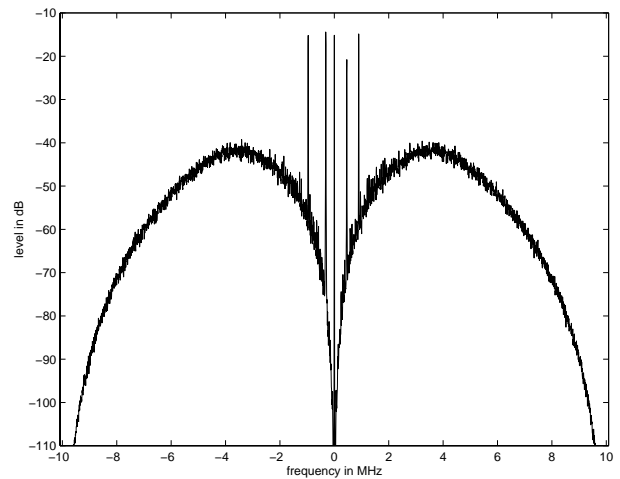


Fig. 5: Multiplier free modified CIC-filter



a) $\Sigma\Delta$ modulated input signal, $f_{in} = 25$ MHz



b) $N_I = 1$, $N_D = 3$, $K = 2$, $L = 46$, $M = 57$, $f_{out} \approx 20.175$ MHz

Fig. 6: Sample rate conversion with modified CIC-filters and a second order, single stage 1-bit $\Sigma\Delta$ -modulator as ADC (complex input signal)

6. CONCLUSIONS

By realizing anti-alias and anti-image filtering, which is necessary in sample rate adaptation applications, as LPTV-systems, an intermediate clock rate being higher than the input sample rate can be avoided. In contrast to Lagrange interpolators time-variant CIC-filters realize not only anti-image filtering but also anti-alias filtering if required. Both, anti-alias and anti-image filtering, are principally realized in separate sections, enabling an arbitrarily independent choice of the order of the anti-alias filter and the anti-image filter, respectively. Still, both sections are finally implemented in a combined manner. The resulting hardware represents a sample rate converter whose conversion factor can be chosen freely within boundaries imposed by the maximum word length of the registers.

7. REFERENCES

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